REMARKS

At the time of the Office Action dated March 11, 2004, claims 1-6 were pending, all of which stand rejected.

In this Amendment, claims 1-6 have been amended to recite that the claimed method is applied to semiconductor storage devices of common type. Care has been exercised to avoid the introduction of new matter. Adequate descriptive support of this amendment can be found in the specification. For example, on page 7, lines 12-15, it is disclosed that "Tests are performed by means of applying different test patterns to a plurality of semiconductor storage devices under test connected to the tester." On page 3, lines 10-12, the specification discloses that "the speed of change in the threshold values Vth differs from one semiconductor storage device to another." The specification on page 6, lines 15-16 also discloses that regarding Fig. 6, "Reference numeral 66 designates a tolerance of high level; and 67 designates a tolerance of low level." Moreover, on page 7, lines 24-27, it is disclosed that "The method of the present invention is identical with the related-art method in terms of the manner of checking threshold values Vth of the semiconductor storage devices through a lead test." Therefore, it is apparent that the specification discloses "semiconductor storage device of common type" are tested.

Title of the Invention.

The Examiner pointed out that the title of the invention is not descriptive. In response, Applicant has amended the title. Accordingly, withdrawal of the objections to the title of the invention is respectfully solicited.

Claim 1 has been rejected under 35 U.S.C. 112, second paragraph.

The Examiner stated that it is not clear as to how many semiconductor devices there are under test in claim 1. In response, Applicant has amended the preamble of claim 1, as well as those of claims 2-6, for better form. Therefore, Applicant respectfully solicits withdrawal of the rejection of claim 1.

Claims 1-3 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Sugamori in view of Kawaguchi

In the statement of the rejection, the Examiner admitted that Sugamori does not teach "determining whether or not results of the tested semiconductor storage devices fall within a predetermined tolerance," as recited in claim 1. Then, the Examiner asserted that Kawaguchi teaches the missing feature of Sugamori, and concluded that a person having ordinary skill would have been motivated to modify Sugamori's system based on the teaching of Kawaguchi. The Examiner's asserted motivation to modify Sugamori's system is to provide a memory tester which can conduct data analysis at high speed.

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Based on this legal tenet, Applicant submits that the proposed combination of Sugamori and Kawaguchi does not teach or suggest a method of testing semiconductor storage devices of common type including the step of applying different test patterns to the respective semiconductor storage devices, recited in amended claim 1 (emphasis added). In short, the proposed combination does not teach applying different test patterns to respective semiconductor storage devices of common type, recited in claim 1.

Sugamori is directed to a semiconductor memory test system. This system can be configured by freely combining a plurality of tester modules and an algorithmic pattern generator. Sugamori discloses that "two or more test pin groups can perform the test for different devices or different blocks in the device in parallel at the same time" (emphasis added) (column 6, lines 28-35).

Kawaguchi pertains to a testing apparatus for a redundant memory. This reference discloses a process of replacing defective lines with redundant lines: "The possibility of remedy using the redundant lines ... is judged while the test is being conducted, whenever the comparator ... outputs a failure results, and no remedy processing is carried out for any memory for which remedy is judged to be impossible on the basis of the failure pattern and number of failures generated up to that time" (see column 3, lines 36-55).

Based on Applicant's review of Sugamori, it is apparent that the primary reference merely mentions that "two or more test pin groups can perform the test for different devices," but does not teach that the Sugamori system applies different test patterns to respective devices of common type (see column 6, lines 28-35). Kawaguchi is also silent on testing devices of common type, while the reference is mainly directed to a process of replacing defective lines with redundant lines.

Accordingly, the proposed combination of Sugamori and Kawaguchi would not have suggested each and every limitation of claim 1, even if the combination is assumed to be proper. *In re Royka*, 490 F.2d 981. Applicant, therefore, respectfully solicits withdrawal of the rejection of claim 1.

Applicant notes that if an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed.

Cir. 1988). Accordingly, as claim 1 is patentable for the reasons set forth above, it is submitted that dependent claims 2 and 3 which respectively depend from claim 1 are also patentable. The Examiner's additional comments with respect to the claims do not cure the argued fundamental deficiencies of the proposed combination of Sugamori in view of Kawaguchi. Therefore, Applicant respectfully solicits withdrawal the rejection of claims 2 and 3.

Claims 4 and 6 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Sugamori in view of Kawaguchi and White, Jr. et al.; and claim 5 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Sugamori in view of Kawaguchi and Watanabe.

Applicant understands that White, Jr. et al. and Watanabe disclose as follows:

White, Jr. et al. is directed to a method of inspecting semiconductor integrated circuit. The reference discloses applying to each device an electrical test sequence including a plurality of different data input and output patterns for a plurality of different addresses. The plurality of different data input and output patterns include writing ones over zeros and reading the ones, then writing zeros over ones and reading the zeros (see claims 10 and 12).

Watanabe discloses a test method of a nonvolatile semiconductor memory including the steps of disabling a write instruction directing a pre-erase data write, and executing a one-time test data write and subsequent automated data erase according to an erase instructions.

In response, Applicant submits that as independent claim 1 is patentable for the reasons set forth above, it is submitted that dependent claims 4-6 which respectively depend from claim 1 are also patentable. *In re Fine*, 837 F.2d 1071. Applicant notes that as mentioned above, neither

White, Jr. et al. nor Watanabe discloses applying different test patterns to semiconductor storage devices of common type, recited in claim 1.

Therefore, the Examiner's citation of the above two references and additional comments with respect to claims 4-6 do not cure the argued fundamental deficiencies of the proposed combination of Sugamori in view of Kawaguchi. Therefore, Applicant respectfully solicits withdrawal the rejection of claims 4-6.

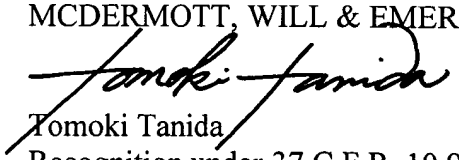
Conclusion.

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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